a semiconductor substrate;

(b) forming a switch element arranged for electrically connecting and disconnecting a semiconductor region formed on said semiconductor substrate and a power supply wiring of the semiconductor device with field effect transistors of predetermined basic cells among said plurality of basic cells; and

(c) forming a plurality of circuits with predetermined basic cells among said plurality of basic cells.

REMARKS

Applicant respectfully requests favorable reconsideration of this application, as amended.

The withdrawal of the restriction requirement is acknowledged with appreciation.

Claims 1 and 39 have been amended and will be addressed later herein. Claims 2-6 have been cancelled without prejudice or disclaimer. Claims 22, 23, and 34 have been revised to address the informalities noted in connection with the rejection under 35 U.S.C. § 112, second paragraph, and to make other editorial changes.

All pending claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Akaogi et al. (Akaogi). Applicant respectfully requests reconsideration and withdrawal of the rejection.

In one of its principal aspects, the present invention provides a semiconductor device and a method of manufacture whereby switch elements (e.g., 3SW1, 3SW2) for switching voltages applied to a semiconductor substrate can be arranged optimally for the design and logical structure of the semiconductor device, that is, without causing a problem in the allocation of components for a main circuit. Switch elements are, more particularly, formed to be included as part of a plurality of cells regularly arranged on the semiconductor substrate which are used to form one or more circuits. By forming the switch elements as parts of cells that are not used in forming the circuit(s), the present invention provides a high degree of freedom in allocation of both the switch elements and elements for constituting the circuit(s). Preferably, a plurality of switch elements are discretely arranged in respective wells to reduce well noise.

Regarding the above aspect of the invention see, for example, lines 12+ in amended Claim 1, lines 12+ in Claim

7, lines 11+ in each of Claims 8-12, lines 12+ in each of Claims 13-14, lines 20+ in each of Claims 28-29, lines 23+ in each of Claims 30-32, lines 15+ in Claim 33, lines 14+ in amended Claim 34, lines 5+ in amended Claim 39, and lines 5+ in each of Claims 40-41.

From another point of view, the switch elements are built into one or more circuits formed of a plurality of basic cells. See lines 12+ in each of Claims 13-14, and lines 8+ in Claim 42.

The cited teachings of Akaogi relate to a memory cell array having drive units 247 and decoding units 241 for decoding multiple signals and accessing the memory cell array. See Figs. 36 and 37. The drive unit 247 has a dual well structure. As described in column 28, this structure resolves a problem that when a negative voltage is applied to the power terminal 250 of the drive unit 247, a junction between a substrate and a diffused layer is forward-biased so that current flows and the output of a specified voltage is disabled. See lines 18-23. Accordingly, the arrangement requires separation of the voltages V_{IN}, V_{IH} applied to the power terminals 252, 254 from the voltages V1, V2 output from the power terminals 250, 251. There is

no suggestion for placing switch elements in basic cells in accordance with Applicant's invention.

It is therefore respectfully submitted that the outstanding rejection on Akaogi should be withdrawn.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully requested,

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Mitchell W. Shapiro

MARKED-UP VERSION OF THE CLAIMS:

1. (Amended) A semiconductor device, comprising:

a semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

power supply wirings arranged for supplying ~~the~~ power supply voltages to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wirings,

wherein said switch elements [are arranged discretely within said semiconductor region] include field effect transistors of said basic cells.

22. (Twice Amended) A semiconductor device as claimed in any one of claims 7 to 12, [wherein] further comprising:

a first wiring layer formed over said switch elements;

a second wiring layer formed over said first wiring

layer and having wiring extending in a direction transverse to wiring of said first wiring layer; and

a third wiring layer formed over said second wiring layer and having wiring extending in a direction transverse to wiring of said second wiring layer,

wherein a wiring electrically connected to [the] gate electrodes of said switch elements is formed of [the] wiring of the third wiring layer and [this wiring is] arranged in parallel to said power supply wirings.

23. (Twice Amended) A semiconductor device as claimed in any one of claims 7 to 14, wherein a semiconductor region for power feeding to supply [the] a predetermined voltage to the semiconductor region formed in said semiconductor substrate is formed in [the] a region between [the] an internal circuit region where a plurality of said basic cells are arranged and [the] a peripheral circuit region at [the] an external side of said internal circuit region.

34. (Amended) A semiconductor device, comprising:

a semiconductor region formed in [the] a peripheral circuit region of a semiconductor substrate;

a plurality of cells for input/output circuits regularly arranged in the peripheral circuit region of said semiconductor substrate;

a plurality of field effect transistors for input/output circuits arranged in each of a plurality of said cells for input/output circuits and formed in said semiconductor region;

power supply wiring arranged for supplying [the] a power supply voltage to a plurality of said field effect transistors for input/output circuits; and

switch elements provided between the semiconductor region in said peripheral circuit region and said power supply wiring,

wherein said peripheral circuit region includes an external region to arrange [said] field effect transistors for input/output circuits of relatively higher threshold voltage and an internal region to arrange [said] field effect transistors for input/output circuits of relatively lower threshold voltage, and

wherein said switch elements [is formed of the] include field effect transistors not used for input circuit among the field effect transistors for input/output circuits in said internal region.

39. (Amended) A method of manufacturing a semiconductor device, comprising [the process of]:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming a switch element arranged for electrically connecting [or] and disconnecting [the] a semiconductor region formed on said semiconductor substrate and [the] a power supply wiring of the semiconductor device with field effect transistors of predetermined basic cells among said plurality of basic cells; and

(c) forming a plurality of circuits with [the] predetermined basic cells among [a] said plurality of [said] basic cells.